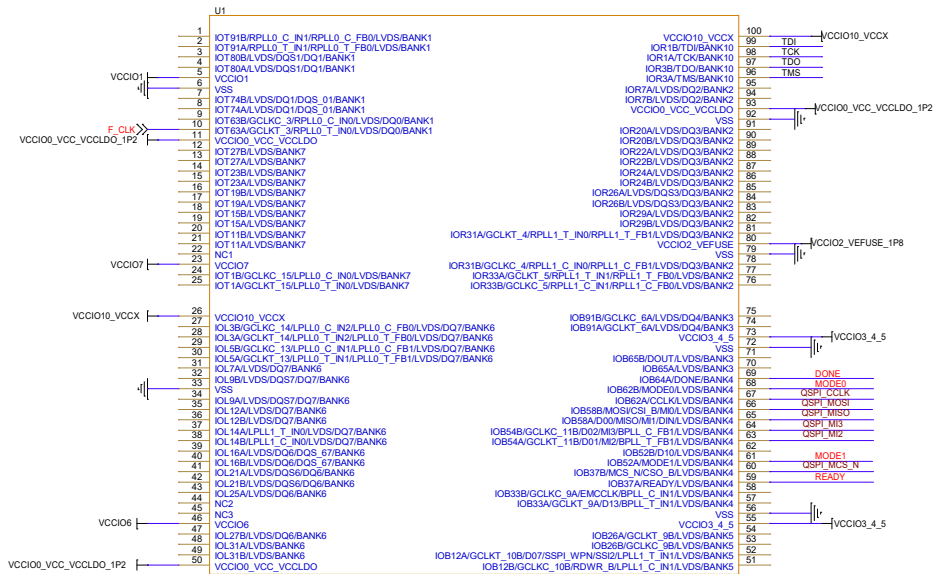
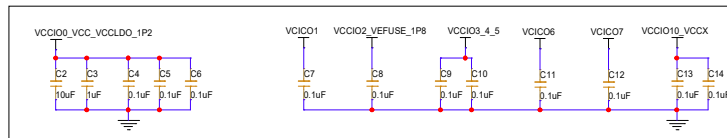


GW5A-EV25LQ100



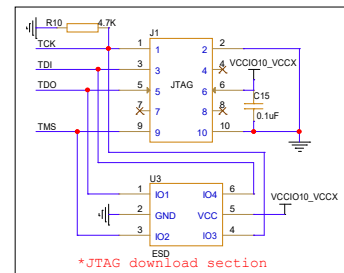
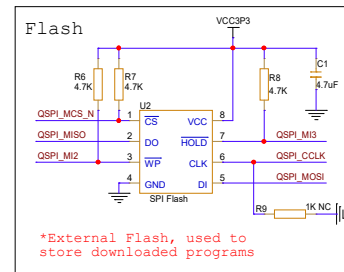
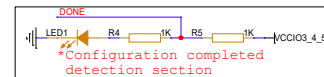
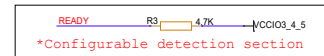
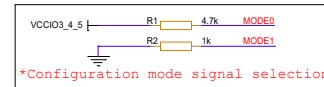
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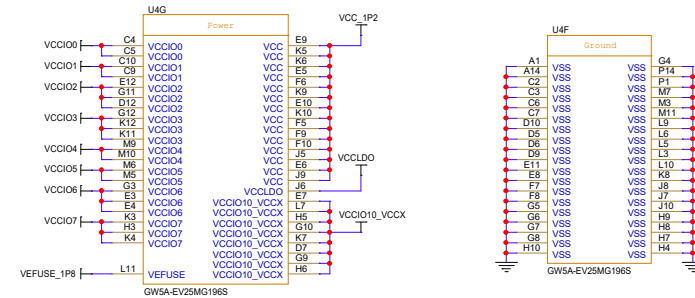
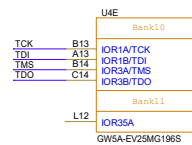
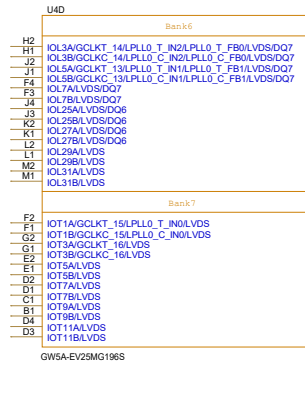
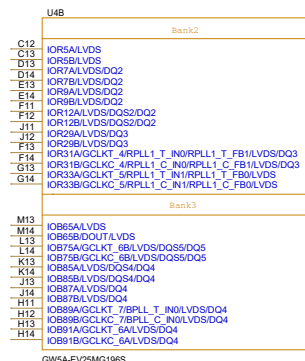
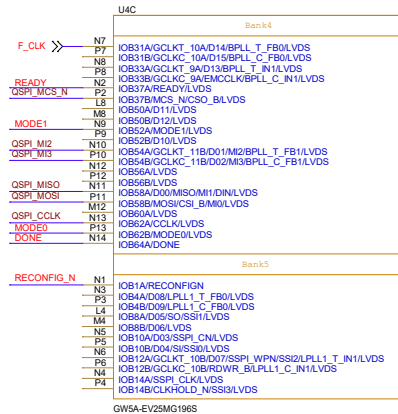
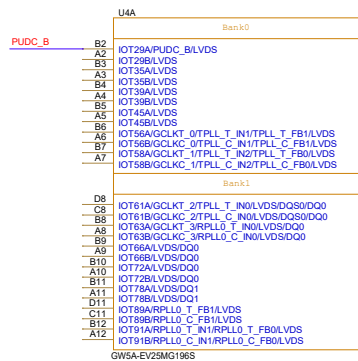
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{GGI}	I/O Bank voltage	1.14V	3.465V
V _{GDK}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDAM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V _{CCDDO} voltage, the higher the power consumption.			
⁽²⁾ When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.



GW5A-EV25MG196S

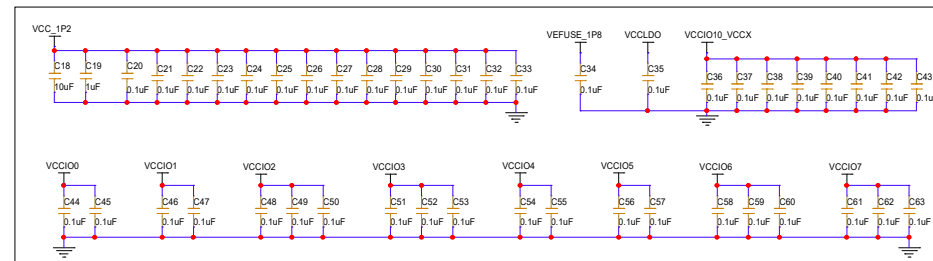
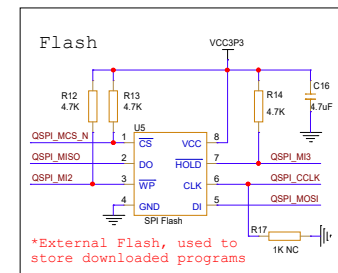
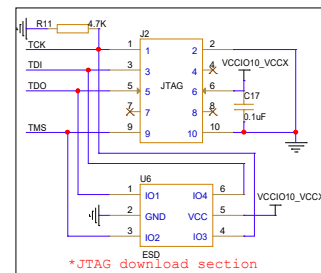


Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CC_LDO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDMM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDMM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V

Note!
^[1] The greater the V_{CCQDO} voltage, the higher the power consumption

⁽²⁾ When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



Notes:

1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. External Flash memory is used to store downloaded programs.

For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

4.VCC core voltage requires a large current, so it is recommended to supply power separately.

5. The MODE pin is the GowinCONFIG configuration mode selection signal

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714.

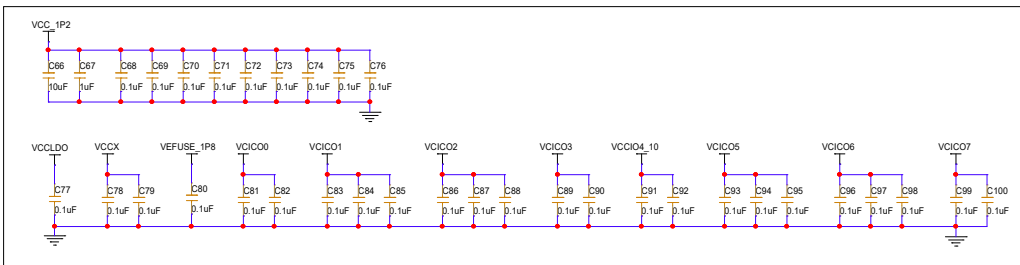
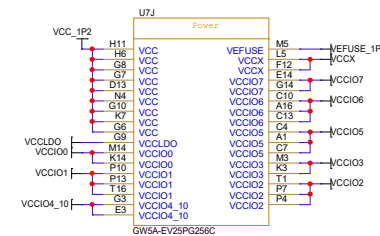
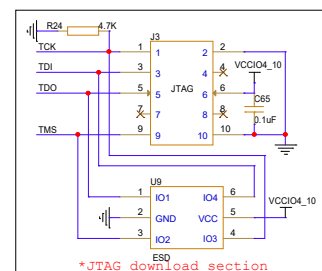
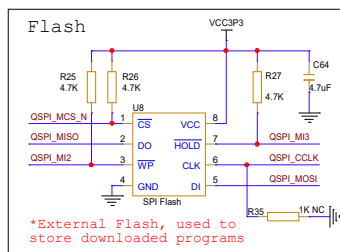
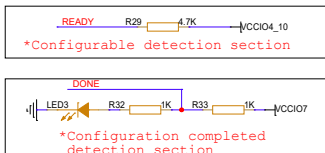
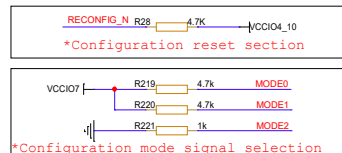
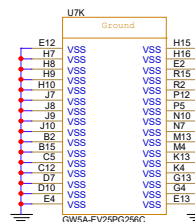
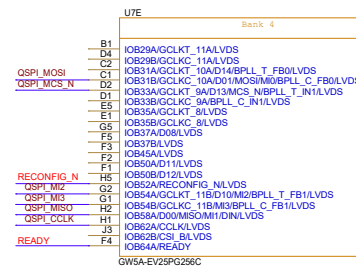
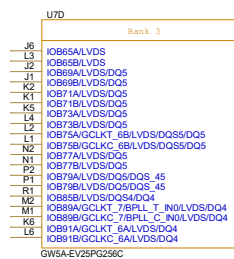
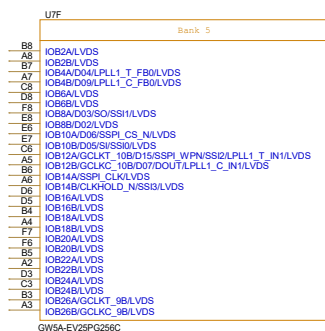
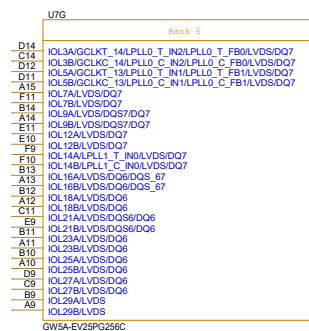
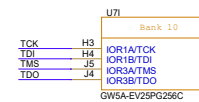
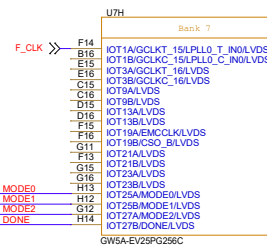
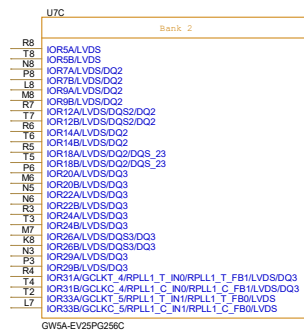
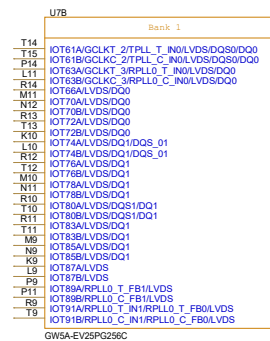
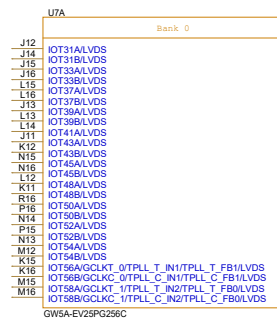
For details about how to select the Mode signal, see Chapter 3.1 of the Arora V 25K FPGA Products Programming and Configuration Guide.

6. The MSPI signal levels must match the Flash power supply voltage.

8. The MSPI signal levels must match the Flash power. If the voltage of the MSPI BANK does not match the

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Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

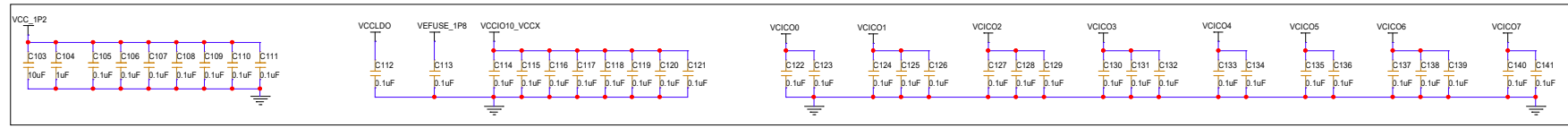
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCO}	Auxiliary voltage	2.375	3.465V
V _{CCOLD} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIP1			
V _{CCDM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDOIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIP1 LP power supply voltage	1.14V	1.32V
Note!			
^[1] The greater the V _{CCOLD} voltage, the higher the power consumption.			
^[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
^[3] If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies.			

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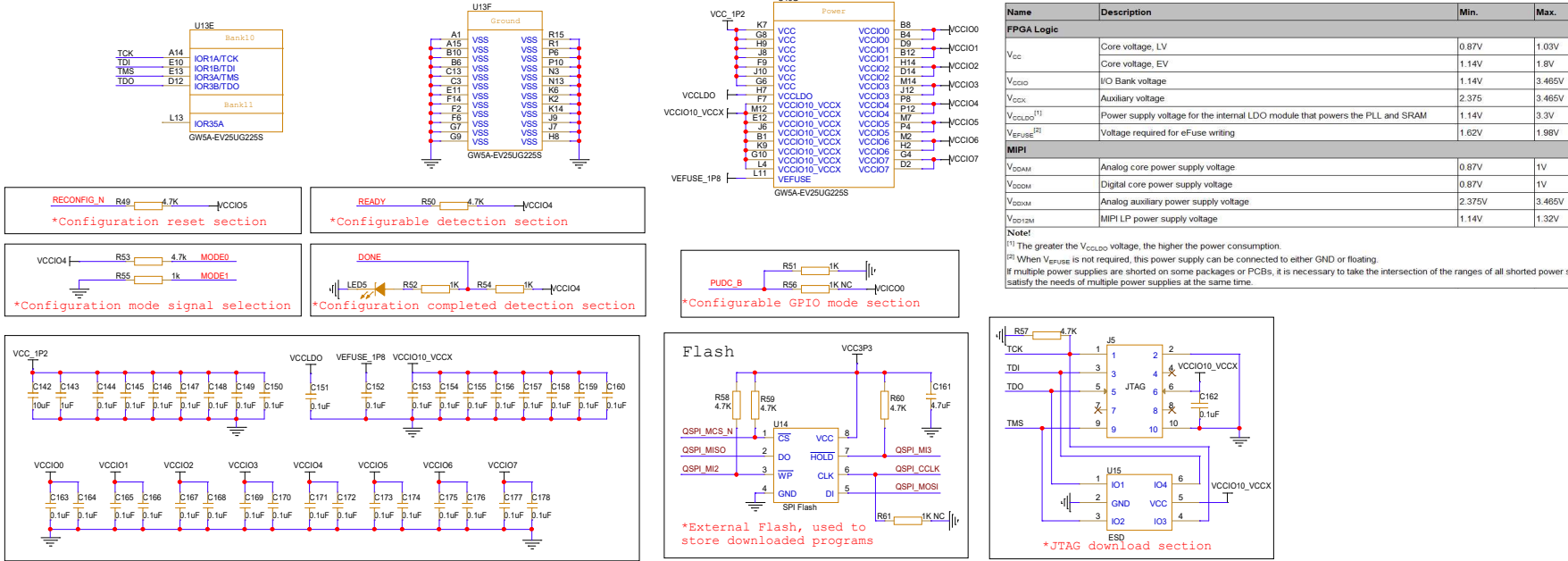
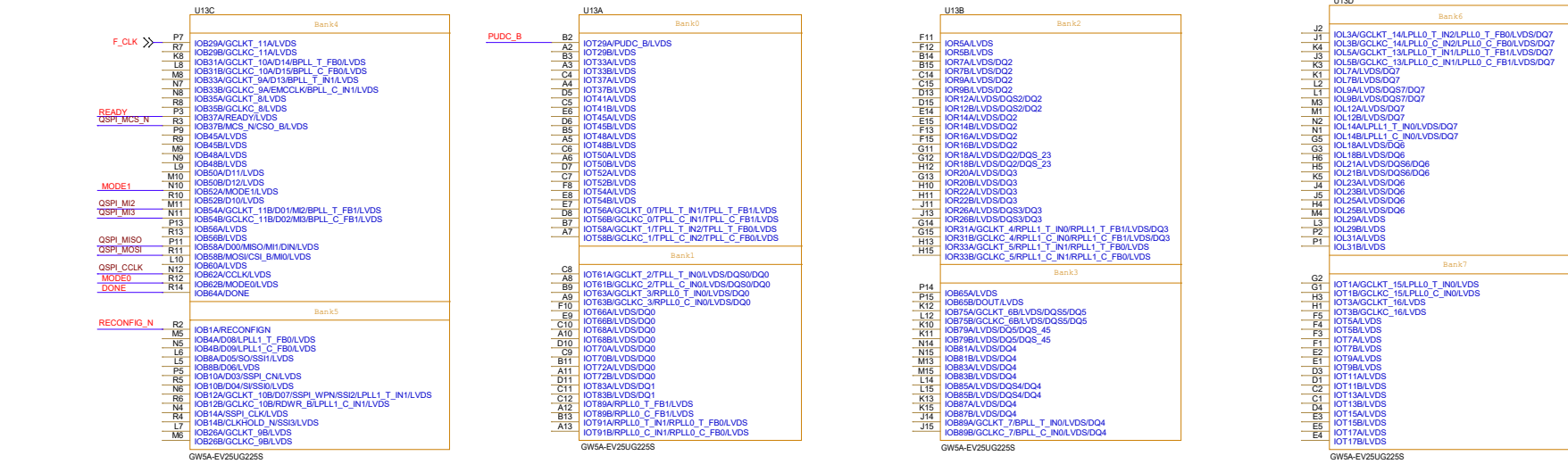
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
[1] The greater the V _{CCDDO} voltage, the higher the power consumption.			
[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies to			



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

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GOWIN Minimum System Diagram			
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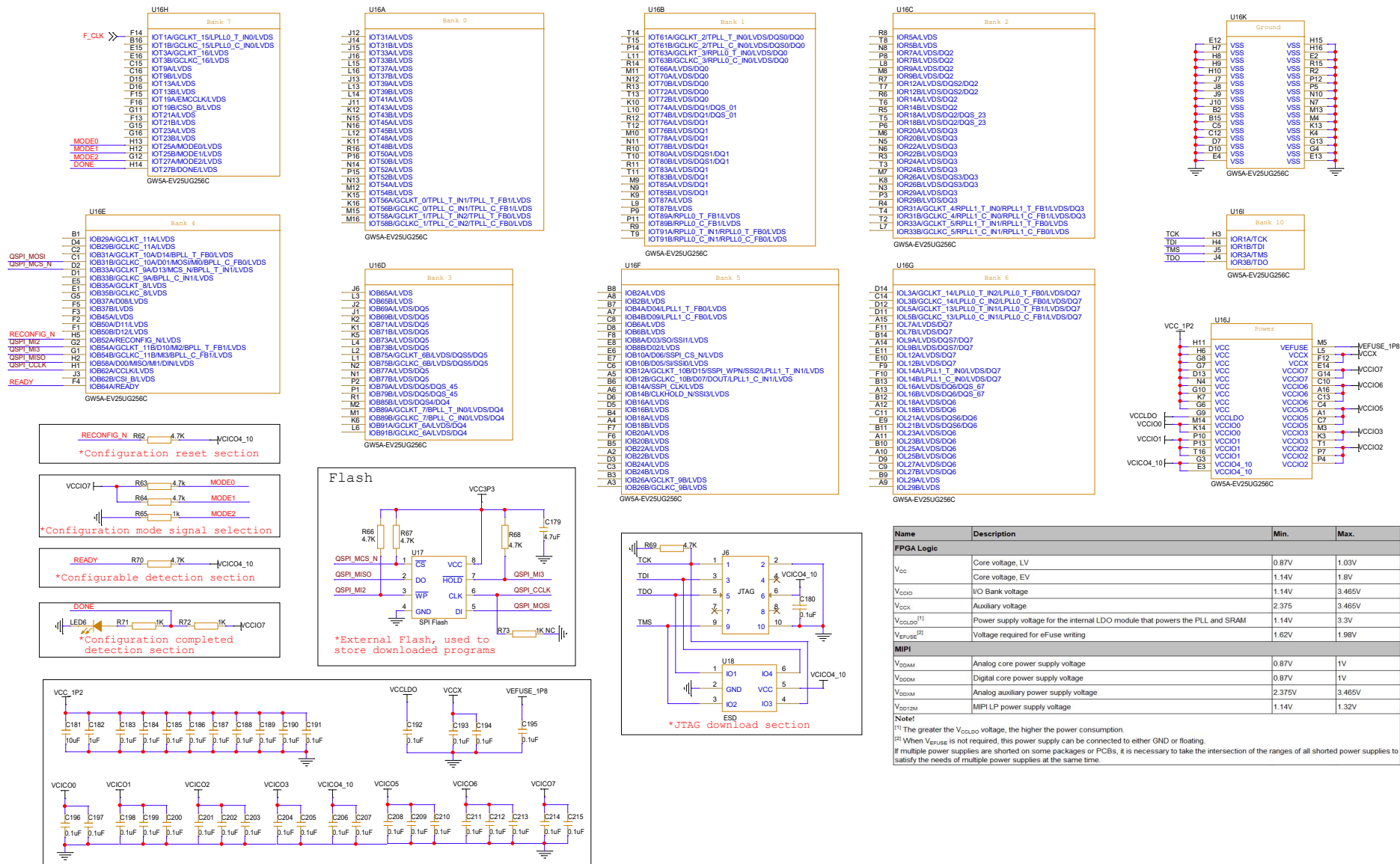
Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCIO0} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDMI}	Analog core power supply voltage	0.87V	1V
V _{DDMI}	Digital core power supply voltage	0.87V	1V
V _{DDMI}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V

Note!
[1] The greater the V_{CCIO0} voltage, the higher the power consumption.
[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

GW5A-EV25UG256C

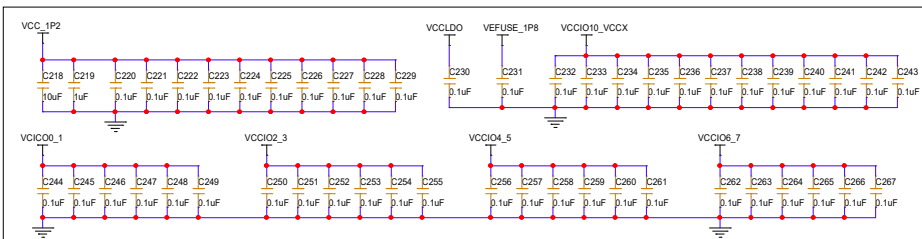
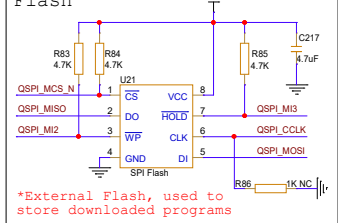
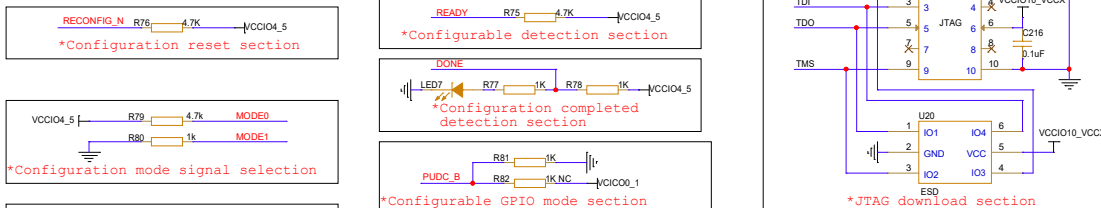


Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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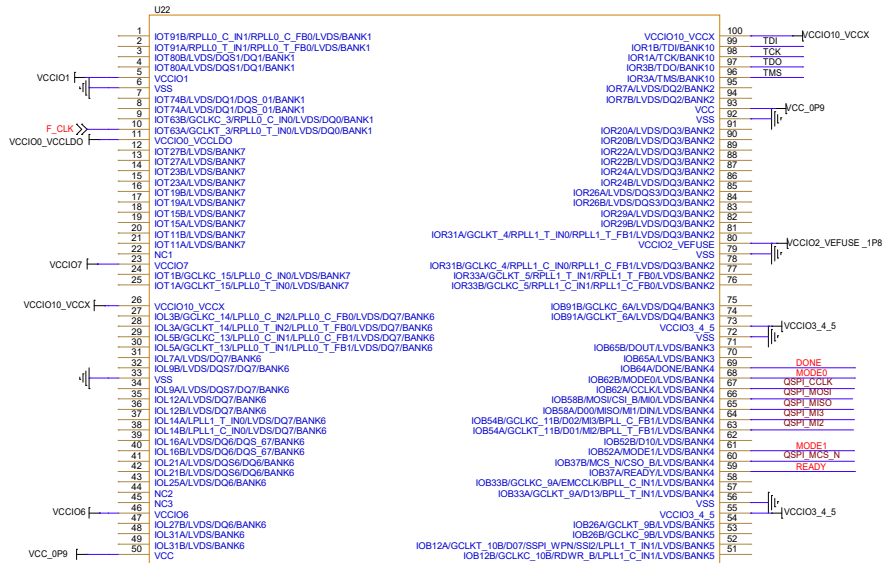


Name	Description	Min.	Max.
PPGA Logic			
V_{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V_{CCK}	I/O Bank voltage	1.14V	3.465V
V_{CCK}	Auxiliary voltage	2.375	3.465V
$V_{CCLDO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{EFUSE}^{(2)}$	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1V
V_{DDCM}	Digital core power supply voltage	0.87V	1V
V_{DDMM}	Analog auxiliary power supply voltage	2.375V	3.465V
V_{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V_{CCLDO} voltage, the higher the power consumption.			
⁽²⁾ When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			

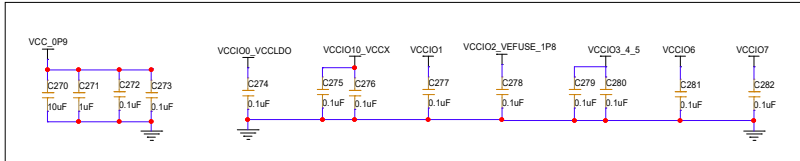
Notes:

- 1.F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

GW5A-LV25LQ100



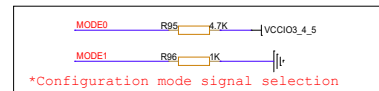
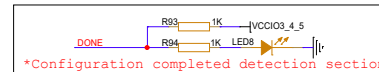
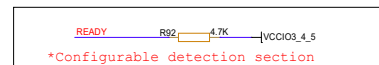
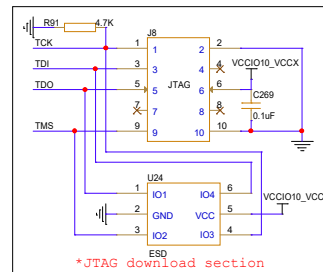
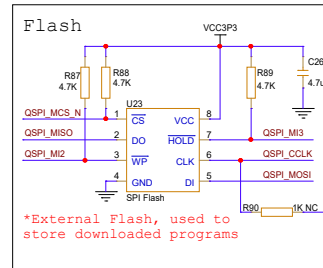
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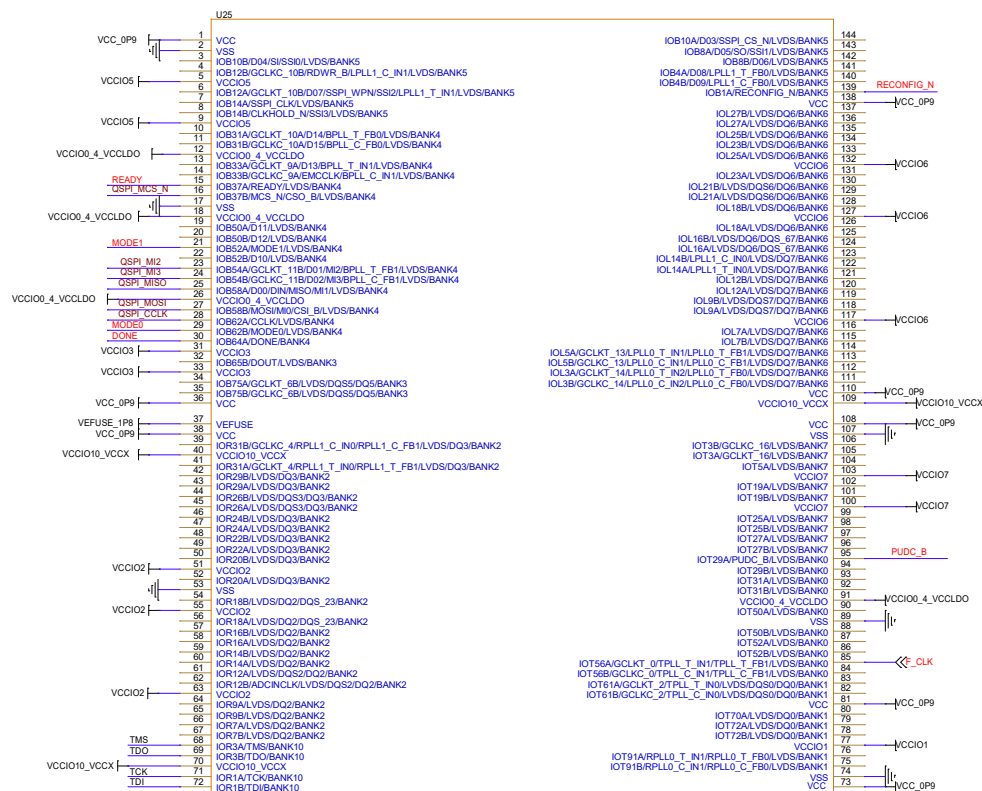
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CGO}	I/O Bank voltage	1.14V	3.465V
V _{GCK}	Auxiliary voltage	2.375	3.465V
V _{CDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Notes			
[1] The greater the V _{CDDO} voltage, the higher the power consumption.			
[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to ensure the correct voltage.			

Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.



GW5A-LV25LQ144

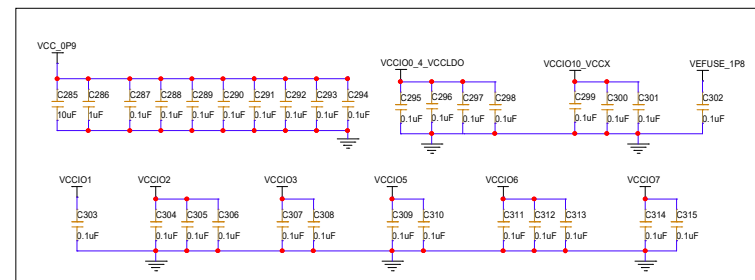
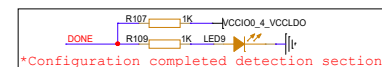
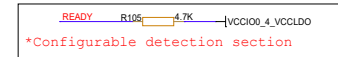
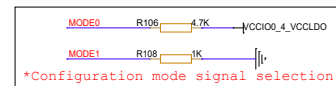
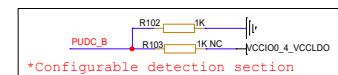
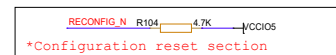
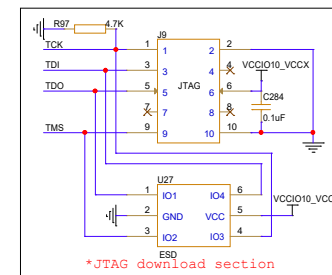
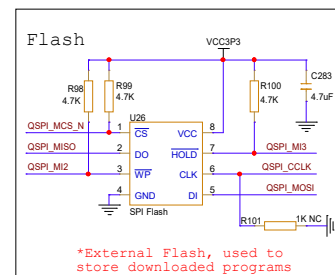


GW5A-LV25LQ144

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V_{CCIO}	I/O Bank voltage	1.14V	3.465V
V_{CCX}	Auxiliary voltage	2.375	3.465V
$V_{CCDDO}^{(1)}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{EFUSE}^{(2)}$	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1V
V_{DDDM}	Digital core power supply voltage	0.87V	1V
V_{DDXM}	Analog auxiliary power supply voltage	2.375V	3.465V
V_{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note:			
⁽¹⁾ The greater the V_{CCDDO} voltage, the higher the power consumption.			
⁽²⁾ When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of all shorted power supplies to meet the needs of multiple power modules at the same time.			

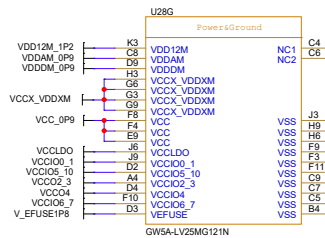
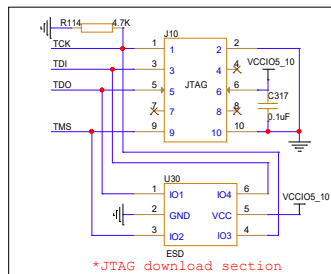
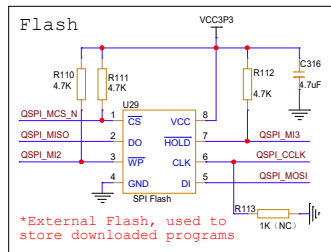
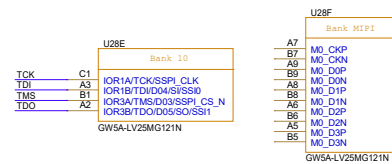
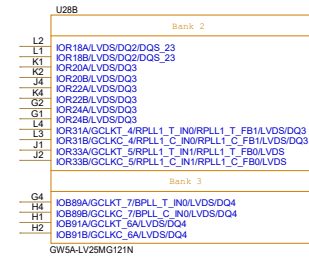
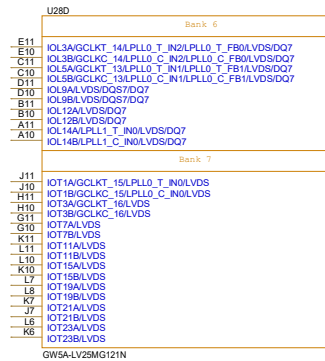
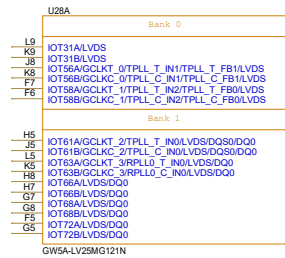
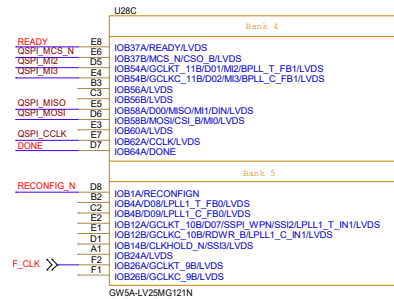
Notes:

1. F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. External Flash memory is used to store downloaded programs.
- For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.
5. The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode pin, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
6. The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

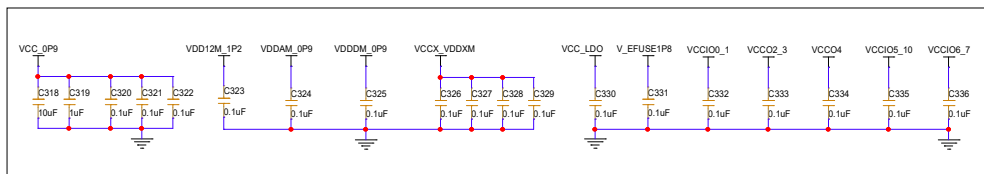


Title				
GOWIN Minimum System Diagram				
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Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCA}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EUFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analogue core power supply voltage	0.87V	1V
V _{DDCM}	Digital core power supply voltage	0.87V	1V
V _{DDIM}	Analogue auxiliary power supply voltage	2.375V	3.465V
V _{DDI2M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
^[1] The greater the V _{CCDDO} voltage, the higher the power consumption.			
^[2] When V _{EUFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.			

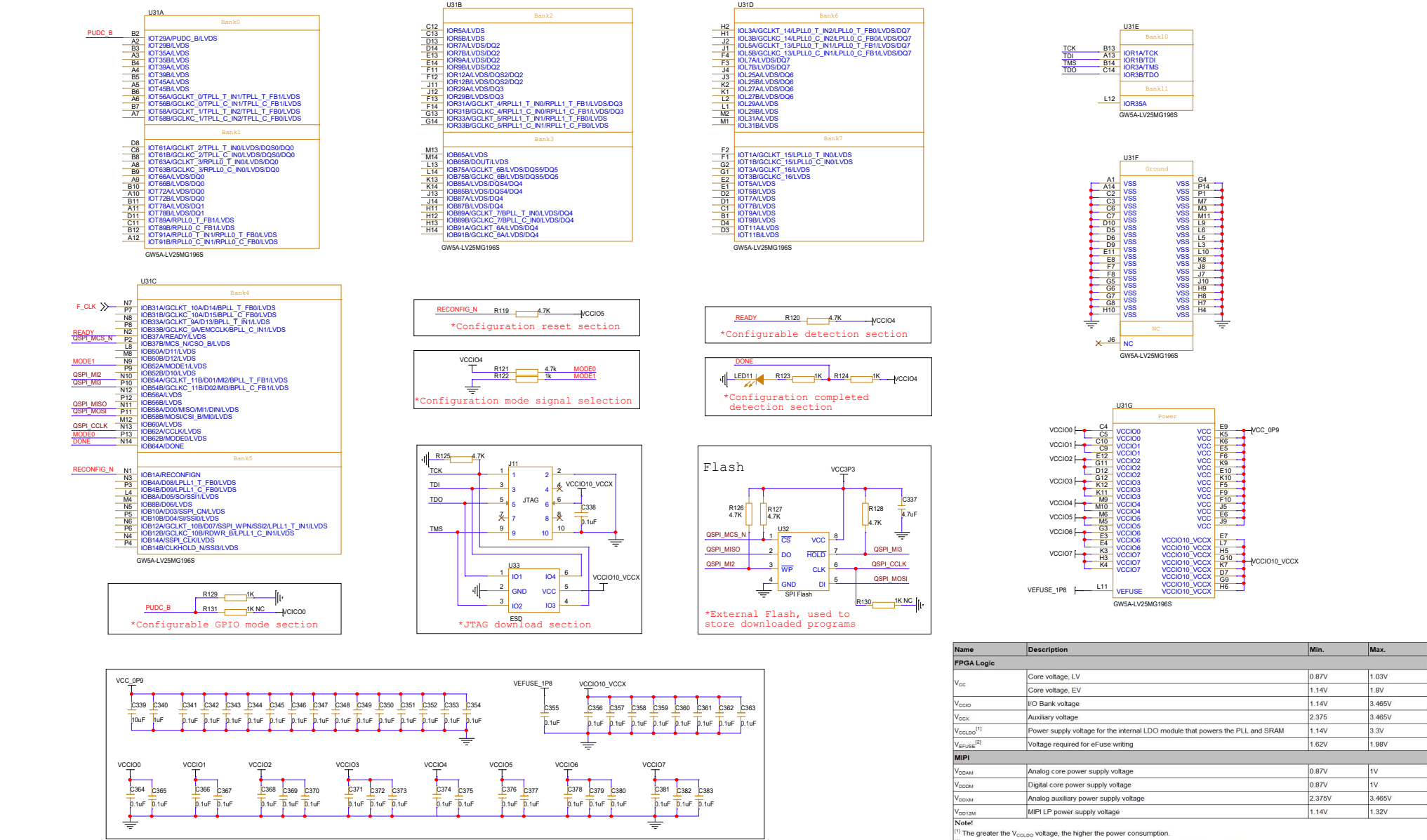


Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Title			
GOWIN Minimum System Diagram			
Size C	Document Number GW5A-LV25MG121N		Rev 2.8
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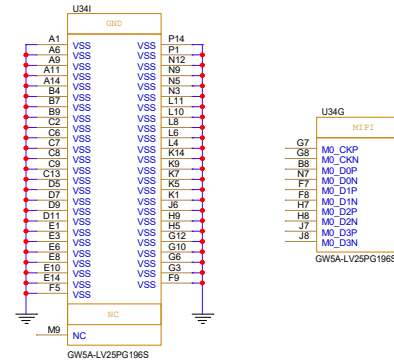
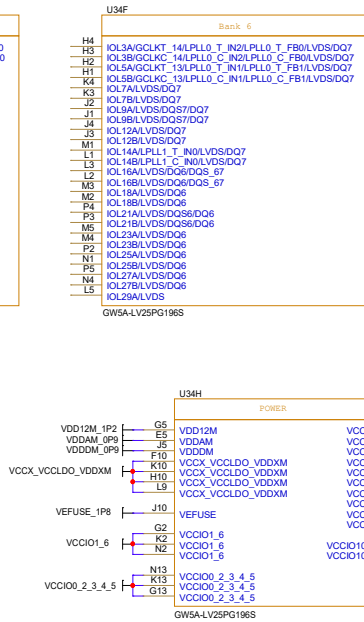
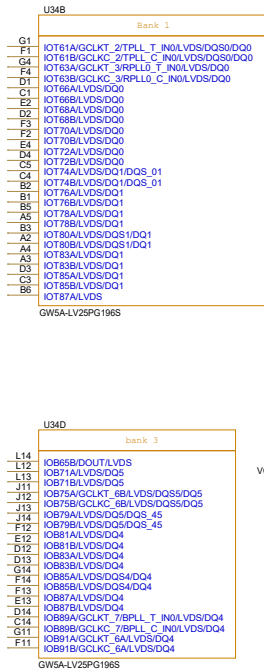
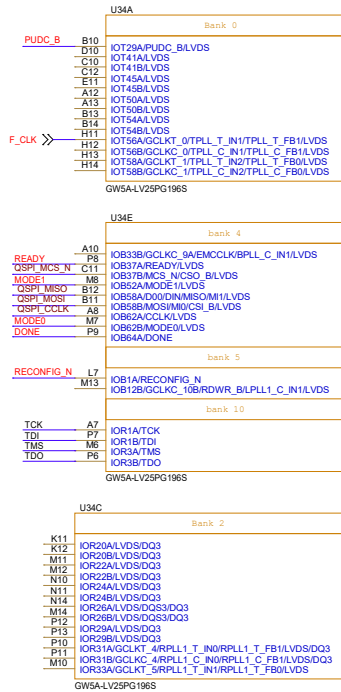


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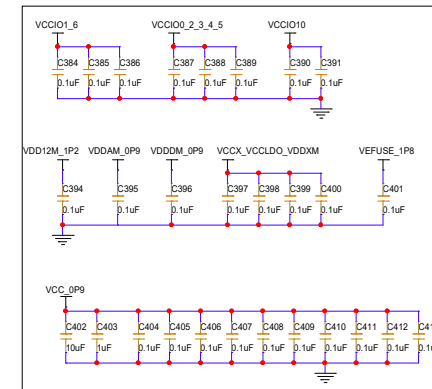
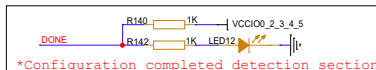
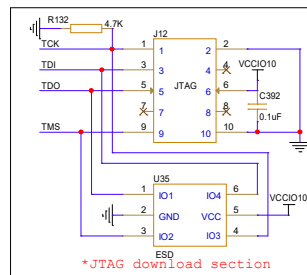
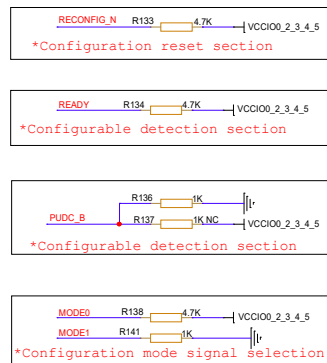
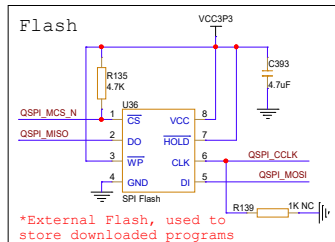
- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs. For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal. For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage. If the voltage of the MSPI Bank does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CCIO}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCLOD} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
[1] The greater the V _{CCLOD} voltage, the higher the power consumption.			
[2] When V _{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			

GW5A-LV25PG196S



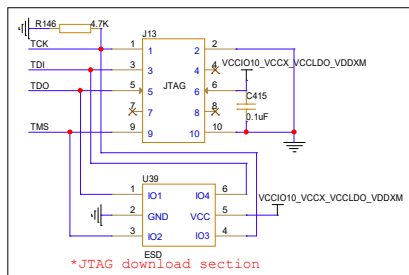
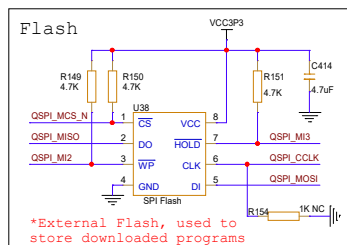
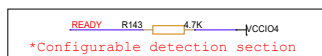
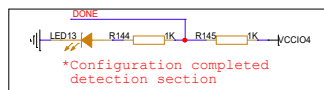
Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V_{CCIO}	I/O Bank voltage	1.14V	3.465V
V_{DDK}	Auxiliary voltage	2.375	3.465V
$V_{CCDDO}^{[1]}$	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
$V_{EFUSE}^{[2]}$	Voltage required for eFuse writing	1.62V	1.98V
MIP1			
V_{DDM1}	Analog core power supply voltage	0.87V	1V
V_{DDDM1}	Digital core power supply voltage	0.87V	1V
V_{DDM1}	Analog auxiliary power supply voltage	2.375V	3.465V
V_{DD12M1}	MIP1 LP power supply voltage	1.14V	1.32V
Note1			
[1] The greater the V_{CCDDO} voltage, the higher the power consumption.			
[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

GW5A-LV25PG256



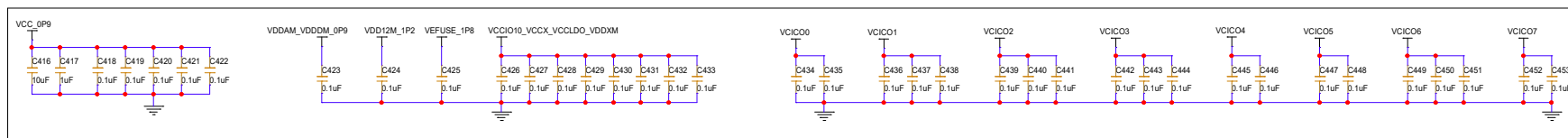
Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCUX}	Auxiliary voltage	2.375	3.465V
V _{CCDDIO} ⁽¹⁾	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ⁽²⁾	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDUXM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V

Note!

⁽¹⁾ The greater the V_{CCDDIO} voltage, the higher the power consumption.

⁽²⁾ When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.

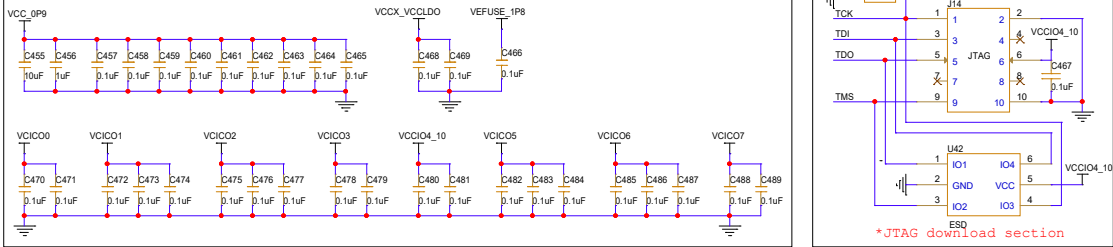
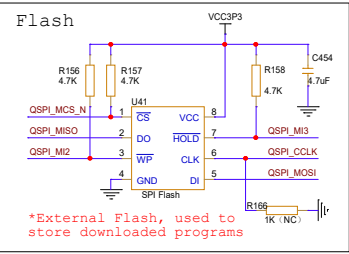
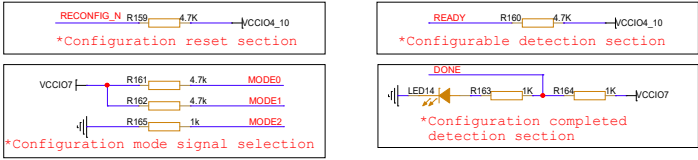
If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.



Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash Model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage,
a level shifter is required for voltage translation.

GW5A-LV25PG256C



Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
V _{CC}	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCX}	Auxiliary voltage	2.375	3.465V
V _{CCDDO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{EFUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.96V
MIPI			
V _{DDAM}	Analog core power supply voltage	0.87V	1V
V _{DDDM}	Digital core power supply voltage	0.87V	1V
V _{DDAM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{DD12M}	MIPI LP power supply voltage	1.14V	1.32V

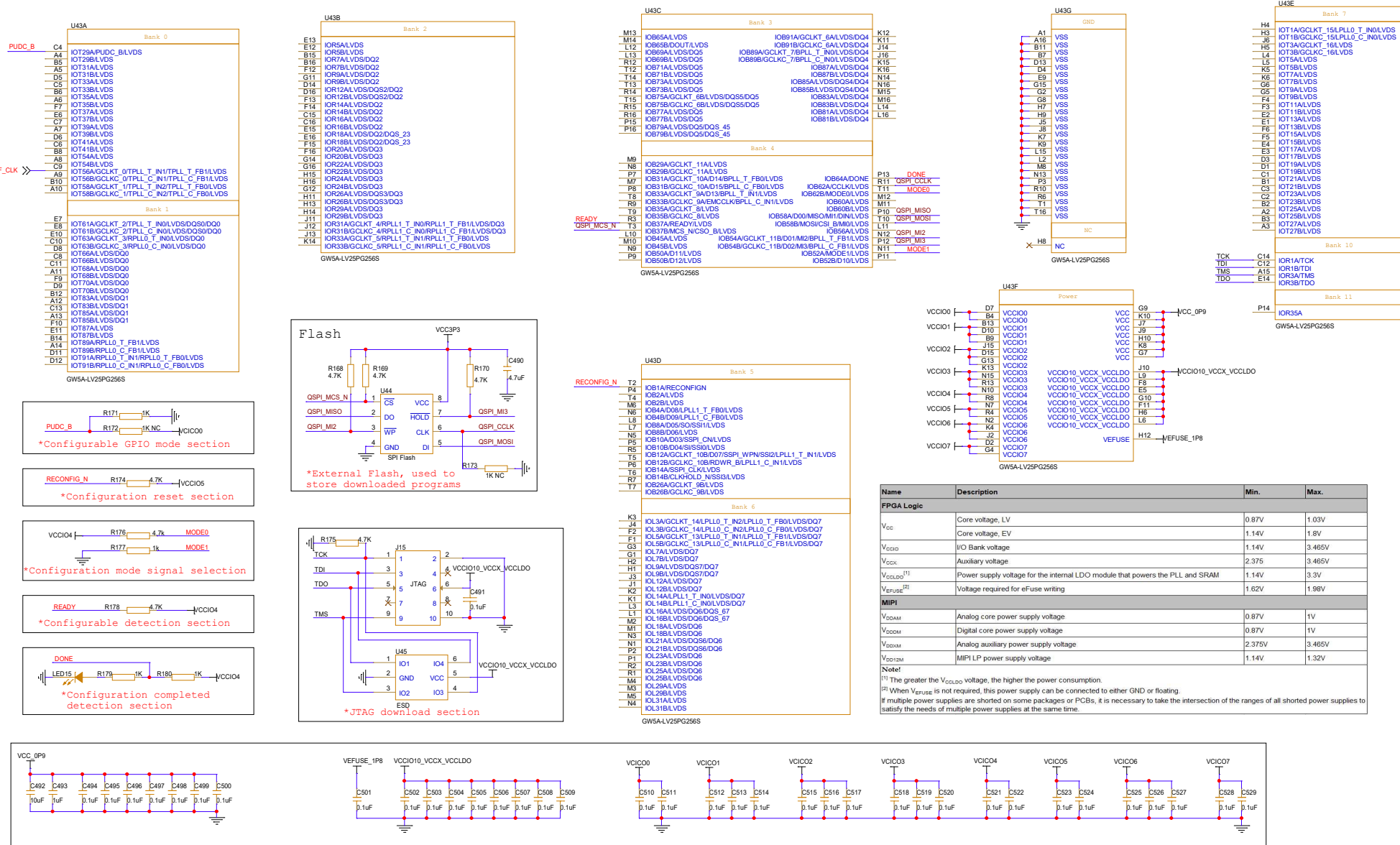
Note:

[1] The greater the V_{CCDDO} voltage, the higher the power consumption.

[2] When V_{EFUSE} is not required, this power supply can be connected to either GND or floating.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

GW5A-LV25PG256S

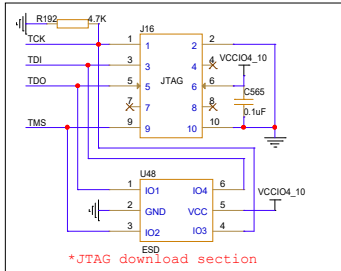
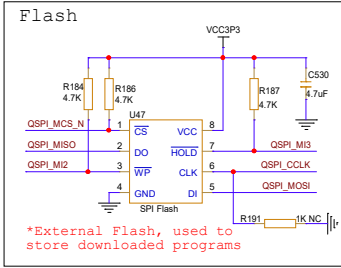
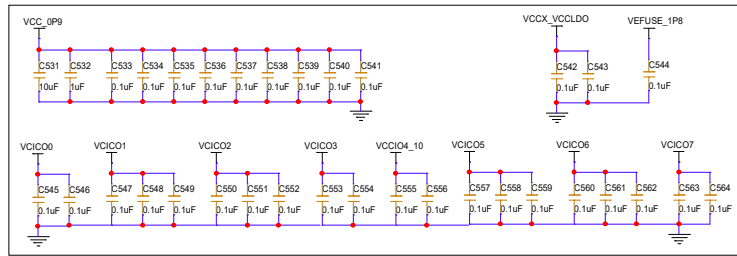
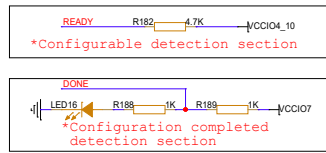
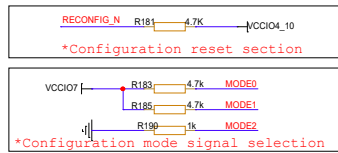
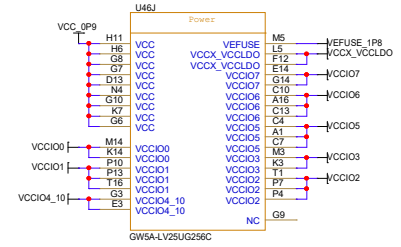
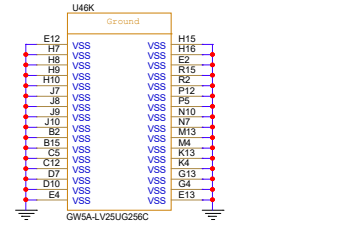
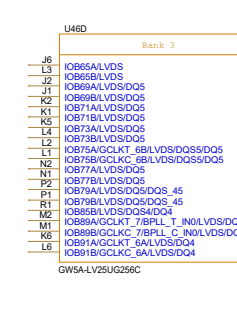
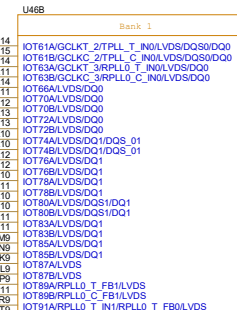
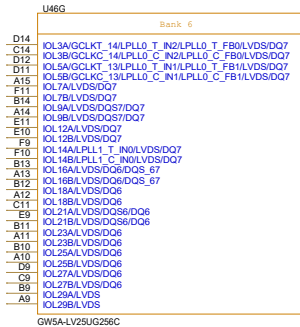
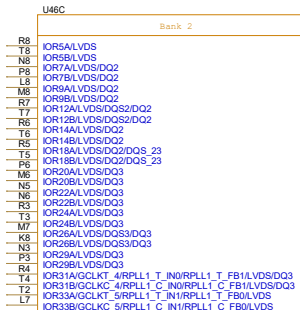
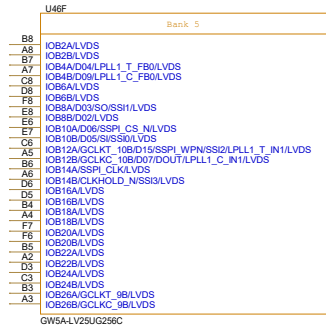
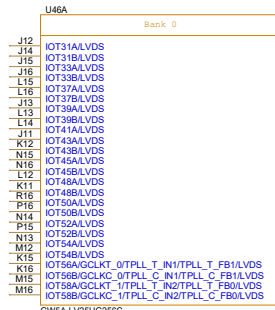
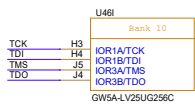
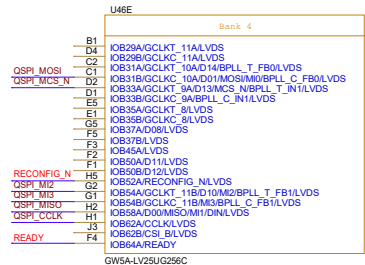
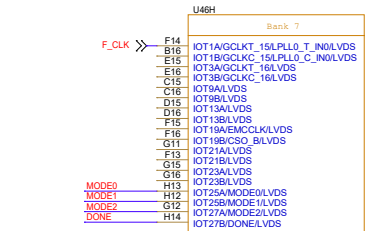


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide .
- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- 6.The MSPI signal levels must match the Flash power supply voltage.
If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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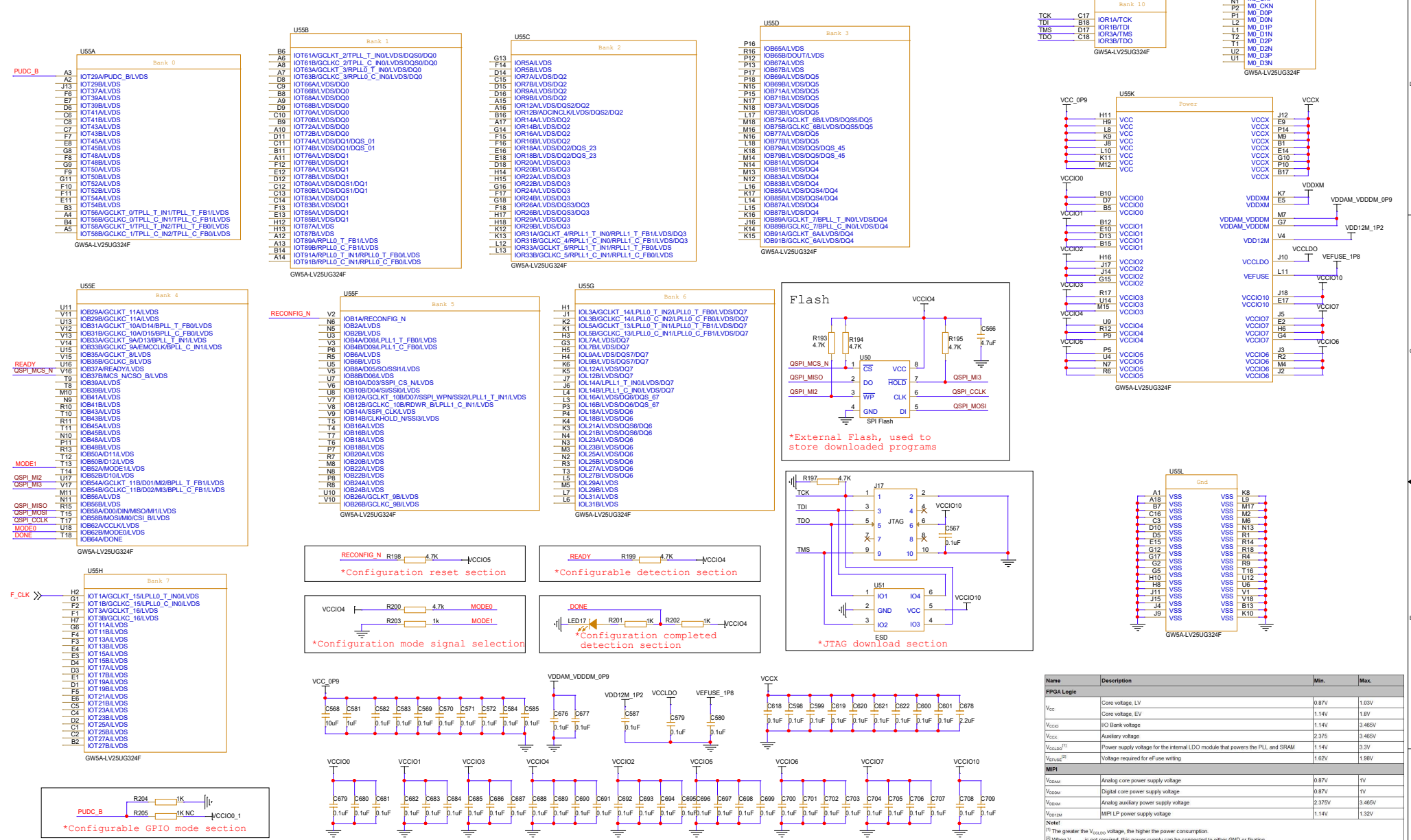


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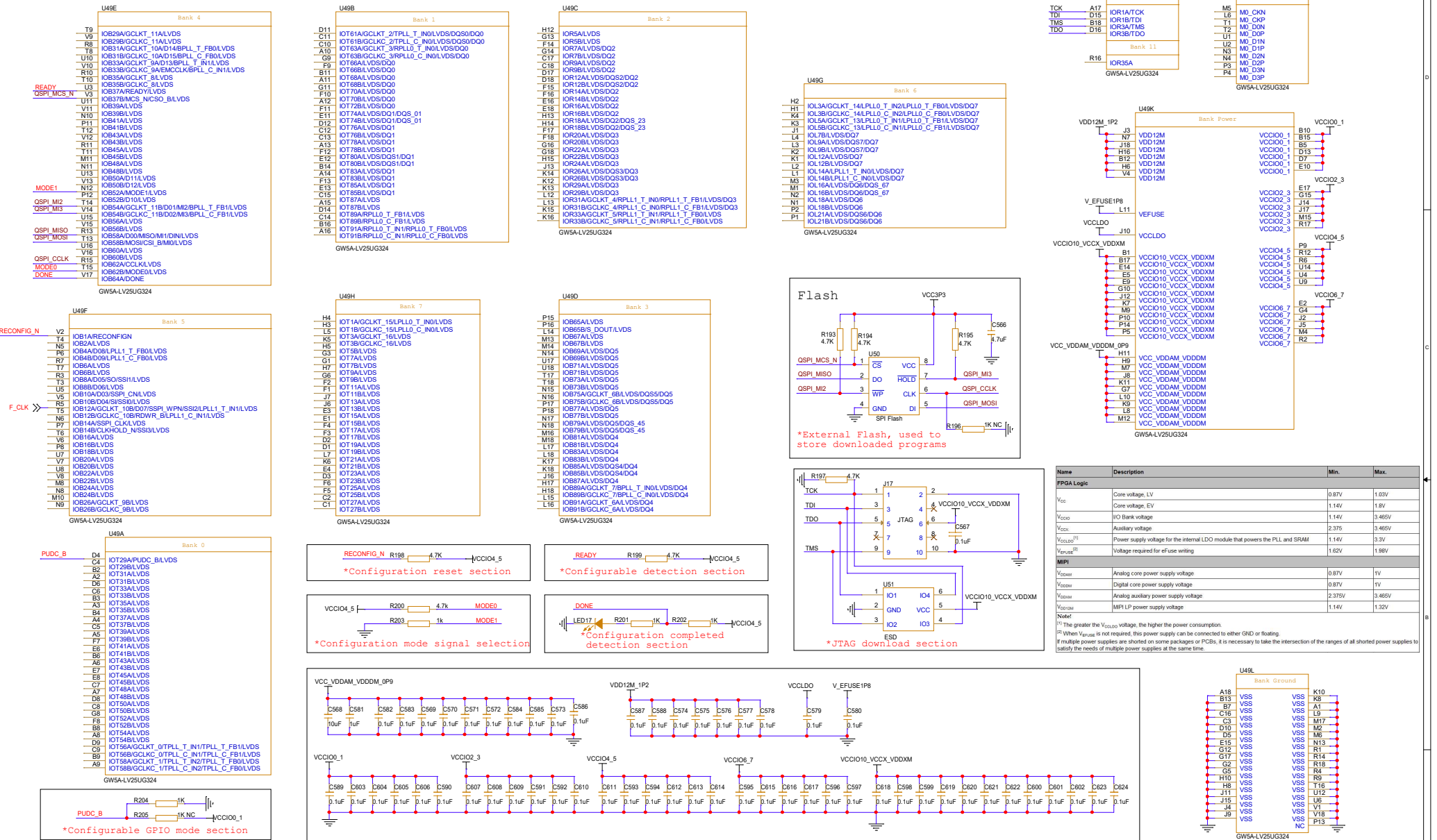
- F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG714, Arora V 25K FPGA Products Programming and Configuration Guide.
- The MSPI signal levels must match the Flash power supply voltage.
- If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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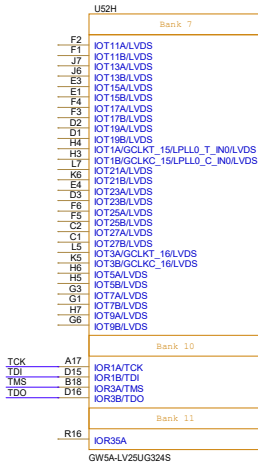
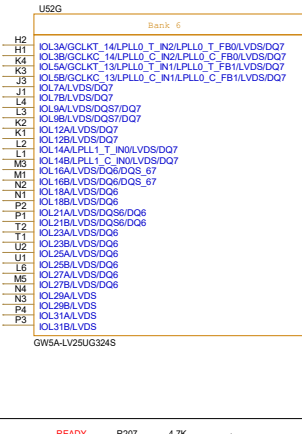
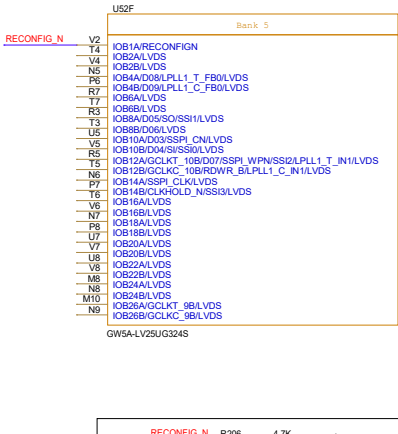
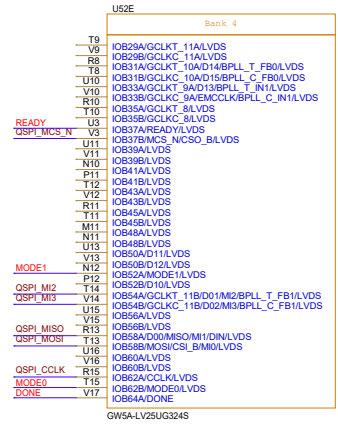
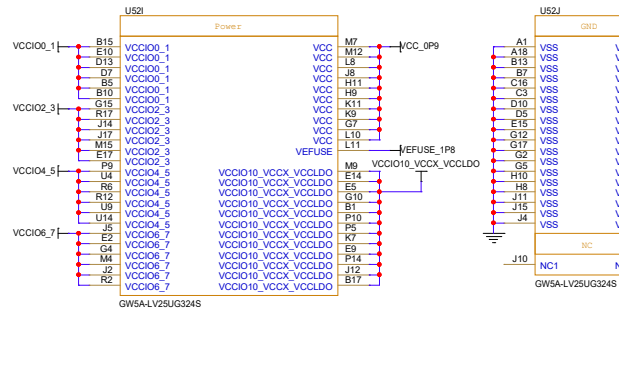
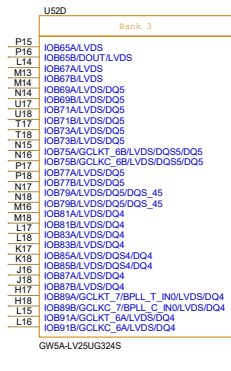
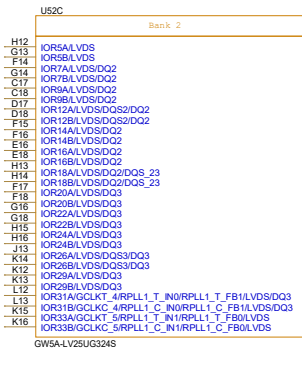
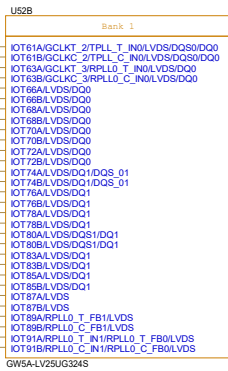
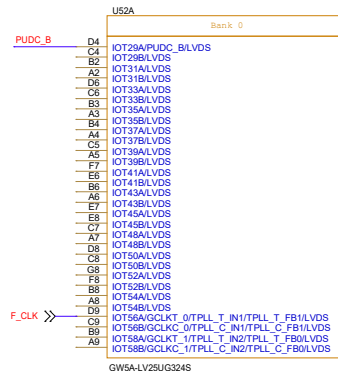
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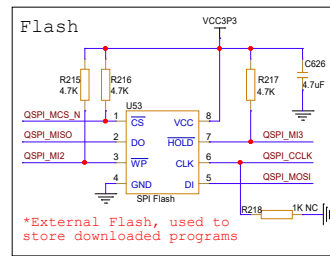
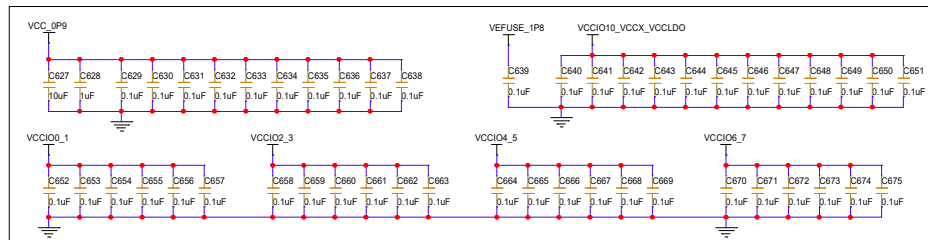
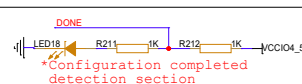
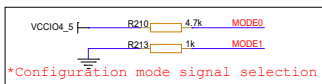
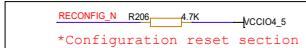
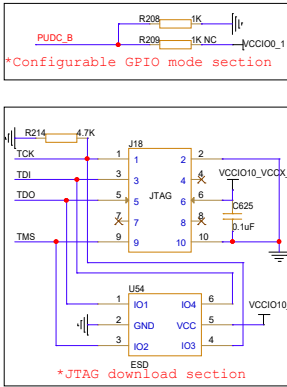
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Name	Description	Min.	Max.
FPGA Logic			
V _{CC}	Core voltage, LV	0.87V	1.03V
	Core voltage, EV	1.14V	1.8V
V _{CCIO}	I/O Bank voltage	1.14V	3.465V
V _{CCUX}	Auxiliary voltage	2.375V	3.465V
V _{CCOLO} ^[1]	Power supply voltage for the internal LDO module that powers the PLL and SRAM	1.14V	3.3V
V _{ERUSE} ^[2]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V _{CCDM}	Analog core power supply voltage	0.87V	1V
V _{CCDM}	Digital core power supply voltage	0.87V	1V
V _{CCDM}	Analog auxiliary power supply voltage	2.375V	3.465V
V _{CC12M}	MIPI LP power supply voltage	1.14V	1.32V
Note!			
^[1] The greater the V _{CCOLO} voltage, the higher the power consumption.			
^[2] When V _{ERUSE} is not required, this power supply can be connected to either GND or floating.			
If multiple power supplies are shared on some packages or PCBs, it is necessary to take the intersection of the ranges of all shared power supplies to satisfy the needs of multiple power supplies at the same time.			



*External Flash, used to store downloaded programs

Notes:

- 1.F.CLK signal is an external input clock signal. It is recommended that F.CLK signal be provided through an active oscillator crystal.
- 2.External Flash memory is used to store downloaded programs.

For details about SPI Flash mode selection, see "Chapter 4.5 SPI Flash Selection" in Arava V 25K FPGA Products Programming and Configuration Guide .

- 3.It is recommended that add an ESD protection chip to the JTAG download circuit.
- 4.VCC core voltage requires a large current, so it is recommended to supply power separately.
- 5.The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in Arava V 25K FPGA Products Programming and Configuration Guide .

- 6.The MSPI signal levels must match the Flash power supply voltage.

If the voltage of the MSPI BANK does not match the Flash power supply voltage, a level shifter is required for voltage translation.

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